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10/542,854	01/09/2006	Yukinobu Sugiyama	046124-5398	7325

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DRINKER BIDDLE & REATH
ATTN: INTELLECTUAL PROPERTY GROUP
ONE LOGAN SQUARE
18TH AND CHERRY STREETS
PHILADELPHIA, PA 19103-6996

EXAMINER	
ELLIS, SUEZU Y	
ART UNIT	**PAPER NUMBER**
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,854	SUGIYAMA ET AL.	
	Examiner	Art Unit	
	Suezu Ellis	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005 and 09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2005 and 09 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/11/05, 8/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on July 11, 2005 and August 16, 2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claim 3 is objected to because of the following informalities:

In claim 3, lines 35-36, claim language recites "a minimum value of respective voltages". It appears claim language should recite "a minimum value of *the* respective voltages" for proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 3, lines 3-4, claim language recites "one pixel is constructed by arranging a plurality of photosensitive portions". However in lines 7-14, claim language recites "one set of the photosensitive portions constitute a plurality of pixels" and "the other set of photosensitive portions constitute a plurality of pixels". Therefore, it is unclear how a subset of the plurality of photosensitive portions from lines 3-4 can constitute a plurality of pixels. The various sets/pluralities of photosensitive portions need to be better differentiated with respect to how they are related to a pixel/plurality of pixels. Please clarify.

In claims 1 and 3, lines 7-8, claim language recites "one set of the photosensitive portions in a plurality of photosensitive portions". While "one set of the photosensitive portions" appears to refer back to the photosensitive portions recited in lines 3-4, the "a plurality of photosensitive portions" is confusing. It is unclear if this plurality of photosensitive portions is different from that recited in lines 3-4. Please clarify.

In claims 1 and 3, lines 11-14, claim language recites "the other set of the photosensitive portions in a plurality of photosensitive portions". It is unclear if "a plurality of photosensitive portions" is different from that recited in lines 3-4 and that

recited in lines 7-8. It is also unclear which photosensitive portions the phrase "the photosensitive portions" in "the other set of the photosensitive portions" refers to. Does it refer to the photosensitive portions recited in lines 3-4, the photosensitive portions from the "one set of the photosensitive portions" or the photosensitive portions in "a plurality of photosensitive portions" in lines 7-8? Further, claim language recites the limitation "the other set of the photosensitive portions". The various photosensitive portions need to be better differentiated. There is insufficient antecedent basis for this limitation in the claim. It is unclear what other set applicant is referring to. Perhaps applicant means another set of photosensitive portions. Please clarify.

In claims 1 and 3, lines 7-10, it is unclear if applicant means that photosensitive portions within one set of photosensitive portions are electrically connected to each other or if the plurality of pixels in a first direction are electrically connected to each other. In lines 11-14, it is also unclear if photosensitive portions within another set of photosensitive portions are electrically connected to each other or if the plurality of pixels in a second direction are electrically connected to each other. Please clarify.

In claims 1 and 3, in lines 16-17, 19-20, 30-31 and 33-34, it is unclear how the "one group of photosensitive portions" and "the other group of photosensitive portions" are related to the "one set of the photosensitive portions" and to "the other set of photosensitive portions". Are the groups a subset of the sets? Please clarify. The various photosensitive portions need to be better differentiated from those described in lines 3-14.

Claims 1 and 3, recites the limitation "the other group of photosensitive portions" in lines 30-31 and 33-34. There is insufficient antecedent basis for this limitation in the claim. It is unclear what other group applicant is referring to since only one group is recited in the lines above. Please clarify.

Claims not specifically addressed are indefinite due to their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Sugiyama et al. (WO 03/049190). US Pat. 7,193,197 will be used as an English translation equivalence for WO 03/049190. Hereinafter, Sugiyama et al. will be referred to as Sugiyama.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 1, Sugiyama discloses in Fig. 1 a photodetector (1) comprising a photosensitive region (10) where pixels (11_{mn}) arranged in a two-dimensional array where one pixel is constructed by arranging a plurality of photosensitive portions outputting respective electric currents corresponding to incident light intensities adjacent to each other within a single plane (col. 10, lines 54 – col. 11, line 3). Sugiyama also discloses one set of the photosensitive portions (12_{mn}) constitutes a plurality of pixels arranged in a first direction in the two-dimensional arrangement being electrically connected to each other and another set of the photosensitive portions (13_{mn}) constitutes a plurality of pixels arranged in a second direction in the two-dimensional arrangement being electrically connected to each other (col. 11, lines 4-16). Figs. 13 and 14 illustrate the inclusion of first integrating circuits, a first maximum value detecting circuit, a first A/D converter circuit, second integrating circuits, a second maximum value detecting circuit, and a second A/D converter circuit. Sugiyama discloses first integrating circuits, provided so as to correspond to one group of photosensitive portions electrically connected to each other in the plurality of pixels arranged in the first direction, for converting corresponding electric currents from the one group of photosensitive portions into voltages and outputting the voltages (col. 13, lines 53-58). Sugiyama discloses a first maximum value detecting circuit for detecting a maximum value of the respective voltages outputted from the S/H circuits which are outputted from the first integrating circuits (col. 19, lines 23-25). Sugiyama discloses a

first A/D converter circuit for converting the respective voltages outputted from the first integrating circuits into digital values within an A/D conversion range based on the maximum values detected by the first maximum value detecting circuit and outputting the digital values (col. 28, lines 40-44). Though Sugiyama fails to expressly disclose the A/D conversion range being from the maximum value detected by the first maximum value detecting circuit to a value smaller than the maximum value by a predetermined value, this is considered inherent to the function of an A/D converter – A/D converters inherently have a conversion range where digital values are outputted within that range. Sugiyama also discloses second integrating circuits, provided so as to correspond to the other group of photosensitive portions electrically connected to each other in the plurality of pixels arranged in the second direction, for converting corresponding electric currents from the other group of photosensitive portions into voltages and outputting the voltages (col. 20, line 61 – col. 21, line 10). Sugiyama further discloses a second maximum value detecting circuit for detecting a maximum value of the respective voltages outputted from the second integrating circuits (col. 21, lines 36-38) and Sugiyama also discloses a second A/D converter circuit for converting the respective voltages outputted from the second integrating circuits into digital values within an A/D conversion range based on the maximum values detected by the second maximum value detecting circuit and outputting the digital values (col. 21, line 60 – col. 22, line 9). Though Sugiyama fails to expressly disclose the A/D conversion ranger being from the maximum value detected by the second maximum value detecting circuit to a value

smaller than the maximum value by a predetermined value, this is considered inherent to the function of an A/D converter.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 10 of U.S. Patent No. 7,193,197. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claim 1 of the current application is a broader version of claims 1 and 10 of U.S. Patent No. 7,193,197, as illustrated below.

Claim 1 of the current application with respect to claims 1 and 10 of U.S. Patent No. 7,193,197 is as follows:

A photodetector including a photosensitive region where pixels are arranged two-dimensionally;

one pixel being constructed photosensitive portions outputting a plurality of respective electric currents corresponding to incident light intensities adjacent to each other within a single plane; (col. 26, lines 34-39)

one set of the photosensitive portions *(photosensitive portions on one side)* in a plurality of photosensitive portions *(amongst the plurality of photosensitive portions)* constituting a plurality of pixels arranged in a first direction in the two-dimensional arrangement being electrically connected to each other; (col. 26, lines 40-48)

the other set of the photosensitive portions *(photosensitive portions on the other side)* in a plurality of photosensitive portions *(amongst the plurality of photosensitive portions)* constituting a plurality of pixels arranged in a second direction in the two-dimensional arrangement being electrically connected to each other; (col. 26, lines 49-57)

the photodetector comprising:

first integrating circuits, provided so as to correspond to one group of photosensitive portions electrically connected to each other in the plurality of pixels arranged in the first direction, for converting corresponding electric currents from the one group of photosensitive portions into voltages and outputting the voltages; (col. 28, lines 21-27)

a first maximum value detecting circuit for detecting a maximum value of the respective voltages outputted from the first integrating circuits; (col. 28, lines 37-39)

a first A/D converter circuit for converting the respective voltages outputted from the first integrating circuits into digital values within an A/D conversion range from the maximum value detected by the first maximum value detecting circuit to a value smaller than the maximum value by a predetermined value and outputting the digital values; (col. 28, lines 40-44)

second integrating circuits, provided so as to correspond to the other group of photosensitive portions electrically connected to each other in the plurality of pixels arranged in the second direction, for converting corresponding electric currents from the other group of photosensitive portions into voltages and outputting the voltages; (col. 28, lines 45-51)

a second maximum value detecting circuit for detecting a maximum value of the respective voltages outputted from the second integrating circuits; (col. 28, lines 62-64) and

a second A/D converter circuit for converting the respective voltages outputted from the second integrating circuits into digital values within an A/D conversion range from the maximum value detected by the second maximum value detecting circuit to a value smaller than the maximum value by a predetermined value and outputting the digital values. (col. 28, line 65 – col. 29, line 3)

Claim language of claim 10 of U.S. Patent No. 7,193,197 fails to expressly recite the plurality of photosensitive portions arranged adjacent to each other *within a single plane*. However, claim 10 does recite that the pixels are arranged two-dimensionally, thus the plurality of photosensitive portions is considered to be arranged within a single plane.

Claim language of claim 10 of U.S. Patent No. 7,193,197 fails expressly recite the first maximum value detecting circuit for detects a maximum value of the respective voltages *outputted from the first integrating circuits* and the second maximum value detecting circuit for detects a maximum value of the respective voltages *outputted from the second integrating circuits*. Claim 10 does recite the first maximum value detecting circuit detects maximum values of the voltages from each of the first sample-and-hold circuits and the claim the second maximum value detecting circuit detects maximum values of the voltages from each of the second sample-and-hold circuits. Claim 10 further recites the first sample-and-hold circuits correspond to the first CDS circuits and output the voltages from the first CDS circuits and the first CDS circuits correspond to the first integrating circuits and output voltages from the first integrating circuits. Claim 10 recites the same relationship for the second-sample-and-hold circuits, second CDS circuits, and second integrating circuits. Therefore, the first maximum value detecting circuit is considered to detect a maximum value of the respective voltages outputted from the first integrating circuits and the second maximum value detecting circuit for detects a maximum value of the respective voltages outputted from the second integrating circuits.

Claim language of claim 10 of U.S. Patent No. 7,193,197 fails expressly recite a first A/D converter circuit for converting the respective voltages outputted from the first integrating circuits into digital values within *an A/D conversion range from the maximum value detected by the first maximum value detecting circuit to a value smaller than the maximum value by a predetermined value* and outputting the digital values. However, this is considered inherent to the function of an A/D converter – A/D converters inherently have a conversion range where digital values are outputted within that range.

Allowable Subject Matter

Claims 2-6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to claim 2, prior art fails to teach or reasonably suggest a photodetector comprising a first level shift circuit and a second level shift circuit, in addition to the other limitations of the claim.

With respect to claim 3, prior art fails to teach or reasonably suggest a photodetector comprising a first and second minimum value detecting circuits, in addition to the other limitations of the claim.

Claims not specifically addressed would be allowable due to their dependency.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mizuno (2002/0012058) discloses a solid state imaging device comprising a two-dimensional array of N photodiodes, first integrating circuits, a first maximum value detection circuit, second integrating circuits, a second maximum value detection circuit and an A/D converter. Mizuno fails to disclose sets/groups of photosensitive portions and a second A/D converter.

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suezu Ellis whose telephone number is (571) 272-2868. The examiner can normally be reached on 8:30am-5pm (Monday-Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571) 272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

THANH X. LUU
PRIMARY EXAMINER